REMARKS

Reconsideration and allowance in view of the foregoing amendments and the following remarks are respectfully requested.

Claims 7 and 13 have been amended. Claims 7-13 are pending in this application.

Claim Rejections 35 U.S.C. §102

Claims 7-10 stand rejected under 35 U.S.C. §102(e) as being anticipated by Fang. Applicant traverses the rejection for the following reasons.

It is submitted that Fang at least fails to disclose or suggest the step of patterning and the step of performing recited in claim 7. According to the claimed invention, an insulating film and a second polysilicon film are formed on the entire structure including a cell region and a peripheral circuit region, and the insulating film including an oxide film and a nitride film is formed under the second polysilicon film. Then, the second polysilicon film and the insulating film are patterned so that they can remain in a given region of the cell region and the peripheral circuit region, respectively, as recited in claim 7, as amended. In contrast, according to Fang, an interpoly dielectric layer 322 composed of an insulting material is formed over the surface of the device and patterned to overlay the poly1 floating gate regions 322 in the memory cell region 317 and form a gate oxide layer in the selected gate transistor regions 313, respectively, as illustrated in Figure 9f (please refer column 10, lines 29-34). In other words, the insulating layer 322 remains only in the memory cell region 317 and in the select gate transistor regions 313, not on the peripheral regions. This is more clear referring Figure 9g, wherein, in the peripheral area 314 and 315, a thin gate oxide 336 is formed in the low voltage peripheral region 314 and a thick gate oxide 337 is formed in the high voltage peripheral region 315, instead of the interpoly dielectric layer 322. Therefore, it is clear that Fang neither discloses nor suggests the step of patterning the second

polysilicon film and the insulating films so that they can remain in a given region of the cell region and the peripheral circuit region, respectively.

Further, Fang fails to disclose or suggest the step of performing an impurity ion implantation process for a given region of the semiconductor substrate to form a source region and a drain region, so that a flash memory cell including the tunnel oxide film, the first polysilicon film, the insulating film and the second polysilicon film is formed in the cell region, and a code address memory cell including the insulating film and the second polysilicon film is formed in the peripheral circuit region, as recited in claim 7, as amended. Please note that the insulating film formed in the code address memory cell is the same film as the insulating film formed in the memory cell. In contrast, as set forth above, the interpoly dielectric layer 322 formed in the cell region 317 is different from the gate oxide 336, 337 formed in the peripheral area 314, 315. Therefore, it is clear that Fang also fails to disclose or suggest the step of performing in claim 7.

Therefore, claim 7 and its dependent claims 8-10 are not anticipated by Fang under 35 U.S.C. §102(e).

Claim Rejections – 35 U.S.C. §103

Claims 11-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Fang in view of Sheng et al. Applicant traverses the rejection for the following reasons.

As set forth above, Fang has failed to disclose or teach each and every element of independent claim 7. It is submitted that Sheng et al. does not supply the above-noted deficiencies of Fang. Therefore, claims 11-12, which are dependent on claim 7, are patentable for the reasons discussed above with respect to claim 7, as well as on their own merits.

Applicant submits that claim 13 also recites the step of patterning and the step of performing, which are substantially the same steps as recited in claim 1. Therefore,

Applicant submits that claim 13 is not made obvious over Fang in view of Sheng et al. under 35 U.S.C. §103(a), for the same reasons discussed above with respect to claim 7.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that claims 7-13are now in condition for allowance and a notice to that effect is earnestly solicited. If any issues remain to be resolved, the Examiner is cordially invited to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

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Date: April 21, 2006